NEWS RELEASE

NTT

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NTT Develops World's First Single-chip MPEG-2 HDTV CODEC LSI -- Enables smaller sizes and greater economy in HDTV CODEC system devices --

Nippon Telegraph and Telephone Corp. (NTT; Head office: Chiyoda-ku, Tokyo; President: Norio Wada) has developed an HDTV[*1] CODEC[*2] LSI construction technology (development code name: VASA [Versatile and Advanced Signal processing Architecture]) to achieve material transmission[*3] in conformance with MPEG-2[*4] international standards. Because huge volumes of calculations are required for the compression and transmission of video images, in the past, several dedicated chips had been used in the process of encoding (compression) and decoding (decompression) HDTV video data based on MPEG-2 standards. Now, for the first time in the world, NTT has achieved this processing on a single chip.
Using this technology, it will be possible to reduce the size of portable HDTV encoder systems to a fraction of the size of the smallest existing units, with an expectation of lower costs as well. With ground wave digital broadcasts scheduled to begin at the end of 2003, the establishment of this broadcast infrastructure, along with smaller and more economical CODEC system devices--which are essential to peripheral installations for these applications--is expected to speed up the arrival of the "digital broadcast society." This technology will not only enable HDTV CODEC processing on a single chip; by using several chips, it will be possible to achieve CODEC processing of large video images surpassing even HDTV, thus opening the door for applications in digital cinema, stereo 3D TV, multi-angle TV, and a wide range of other high-reality large-screen video applications of the future.

○Background to development

For some time now, NTT Cyberspace Laboratories has been developing chips that enable processing of standard TV images (SuperENC) and MPEG-2 encoder boards using these chips, as well as an MPEG-2 portable HDTV encoder system that incorporates nine of these chips. The goal of these development activities is to offer high-quality video distribution and other services that make use of broadband networks.
With the imminent arrival of the "era of HDTV," there is a growing need for smaller and more economical CODEC system devices, and for methods of efficiently providing high-reality large-screen video images that surpass even HDTV, for example in sports broadcasting and live music events. These new technologies will enable the production of richer, more diverse HDTV programming.

○Keys to Related Technologies

1. HDTV CODEC on a single chip (see attached Figs. 1 & 2)
Huge volumes of calculations are required for HDTV CODEC processing. NTT has mounted three encoder cores*5 that operate in parallel onto an IC chip, and has developed a new encoding method (layered parallel encoding) to rapidly supply data to these encoder cores and also to efficiently control the encoding process. Furthermore, by adopting an advanced commercial 0.13 μm CMOS*6 technology, it has integrauted the 60 million transistors required for this operation into a single chip.

2. Using multiple chips to accommodate high-reality, large-screen images that surpass HDTV (see attached Fig. 3)
By incorporating CODEC processing coordination operations and MUX/DEMUX processing into the chips, NTT has achieved CODEC processing of high-reality, large-screen images that surpass HDTV simply by linking several chips, without the need for any specialized external devices.

○Future Developments

In the future, in preparation for the full-scale arrival of the era of HDTV, NTT will work toward the commercialization of these chips and their incorporation into video distribution systems and high-reality, large-screen video systems. It will also work to expand optic networks by promoting the active use of HTV. As part of these activities, it will consider the application of these chips in the high definition CODEC currently under joint development by NHK and NTT Communications. Furthermore, in order to promote the development of diverse services using optic networks, it will aim for further development of the high-compression, high-quality video encoding technologies and LSI architecture technologies that it has been working on up to now, and will continue its work in the development of next-generation CODEC technologies.

<Glossary>

*1: MPEG-2 (Moving Picture Experts Group-2)
MPEG is an international standard related to the compression of video images. MPEG-2 is a standard encoding method for high-quality video, including HDTV and other TV images, and is also used for DVD and digital TV broadcasting.

*2: Material transmission
Material transmission refers to the transmission of video and audio materials to be edited for programs in the broadcast industry. In the case of HDTV, the bitrate used in standard BS digital broadcasting is around 20 Mbps, but even higher rates (between 60 and 150 Mbps) are required for the material transmission level used in the process of producing HDTV programs.

*3: HDTV (High Definition Television)
HDTV is a broadcast method that offers far greater picture and sound quality than standard TV, with more scan lines, wider screens, and the introduction of digital audio.

*4: CODEC (COder and DECoder)
A CODEC device contains the functions of both an encoder (to compress video and audio data into a specified stream) and a decoder (to decompress that video and

audio data from the stream). Because digital video and audio uses huge volumes of data, ti is important to use an appropriate CODEC when compressing data.

*5: Encoder core
This is the basic component used in MPEG-2 video encoding processing; it compresses video information in the specified region.

*6: 0.13 μm CMOS
CMOS is an abbreviation of Complementary Metal Oxide Semiconductor, which is a semiconductor production method characterized by high speeds and low power consumption. Nearly all current semiconductors, from CPUs to memory chips, are manufactured using CMOS. The dimension 0.13 μm represents the current minimum circuit width, making this the most advanced precision process technology in existence.

- Figure 1 Outline of the VASA chip
- Figure 2 HDTV system configuration using VASA chips
- Figure 3 High-reality, large-screen system configuration using VASA

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